

**IS10A
INTEGRATING MULTICHANNEL
SCALER**

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1 IS10A GENERAL DESCRIPTION

The IS10A Integrating Multichannel Scaler is a high speed logical counter and accumulator designed to accumulate high rate events to a selectable number of accumulators associated with a programmable segment of time over multiple iterations. It is intended for use with high event rate sources such as photomultipliers and particle detectors in applications such as photon counting, LIDAR, and spectrometry.

Each iteration, or *cycle*, in the integration process is started by an external signal. Up to 32768 discrete accumulators, or *channels*, are available, each one capable of accumulating a 24-bit (16,777,215) count. The integration time within a channel, or *dwell time*, may be specified to support various count rates or other requirements. The dwell time can be generated internally or externally and can be as little as 250 ns. During a dwell time interval, events from the source device are accumulated as *counts* by one of two 16-bit counters. At the end of the dwell time, the counter contents are added to the channel memory location pointed to by the current channel address and the memory address pointer is incremented to the next channel. This operation is repeated until the specified number of channels have been addressed. Upon reaching the last channel, the IS10A enters an idle state until the next cycle is started by the front panel input. The result of integrating over many cycles is a histogram of counts as a function of the channel address. The signal to noise ratio of the input source will be enhanced due to the statistics of accumulating correlated signals and uncorrelated noise, such as dark counts from a photomultiplier. By using two high speed 16-bit counters in a specially designed “ping-pong” high speed selection scheme, the dead time at the end of a dwell interval is reduced to less than 2 ns. The minimum time between events is less than 1 ns, permitting the IS10A to work at event rates of as much as 1 GHz. The IS10A is designed as a single width CAMAC module with operation determined by commands sent via the CAMAC dataway. These commands are used to specify such parameters as the dwell time and the number of channels per cycle, to set the operating mode, and to read data to a host computer.

The IS10A also includes features which bring additional flexibility to the integration process. The application of a logic signal to the front panel input labeled *Subtract Enable* while the IS10A is integrating causes the dwell interval counts to be subtracted rather than added to the accumulated counts for the currently addressed channel. By synchronizing the *Subtract Enable* signal to a shuttered or chopped signal detector, it is possible to subtract constant noise counts such as dark counts from the signal being observed. This feature may be used to extend the integration time of the system, particularly in cases of high dark count rates. Additionally, the IS10A includes a display generator which permits viewing of memory contents on an X-Y monitor or oscilloscope where the X output corresponds to the channel memory address and the Y output corresponds to the accumulated counts in the associated channel. Finally, an LED array indicator on the front panel can be switch selected to display the current channel address or accumulated counts. This display is used diagnostically to quickly verify the status and correct operation of the integration cycle.

Both TTL level and NIM level event inputs are provided on the IS10A. The TTL input is internally terminated in 470 ohms. The NIM input connector has a 50 ohm termination. The *Channel Increment* (external dwell time input), *Cycle Start*, and *Subtract Enable* inputs are also TTL level signals and are internally terminated in 470 ohms. The X and Y monitor outputs are analog signals with a range of 0 to 5 volts full scale.

1.1 Specifications Summary

General

Dataway Interface

IEEE 583-1975

Ambient Temperature Range

0 to 50 degrees C

Power Requirements

+6 V @ 1.0 A

-6 V @ 2.5 A

+24 V @ 50 mA

-24 V @ 50 mA

Package Size

Single Width CAMAC Module

Features

Memory Size

32768 24-Bit Channels Available

Maximum Accumulated Count

16,772,215 (24-bit)

Dwell Time

External DC to 300 ns

Internal 250 ns to 64 μ s by 250 ns

Maximum Counts Per Dwell Interval

16535 (16-bit)

Cycle Start To First Channel Delay

Less than 50 ns (Internal Timebase)

Maximum Count Rate

1 Billion Counts/Second (1 GHz)

Input Signals

Count Input (NIM) -1.2 V 50 Ω

Count Input (TTL) 2.5 V 470 Ω

Channel Increment (TTL) 2.5 V 470 Ω

Cycle Start (TTL) 2.5 V 470 Ω

Subtract Enable (TTL) 2.5 V 470 Ω

Channel Data Readout

Up To 3 MB/s (Full CAMAC Rate)

Q-Stop Supported

Monitor Outputs

X and Y at 0 - 5 V

Subtract Mode Support

Front Panel TTL Input

Front Panel Analog Display Driver (Monitor Outputs)

X and Y Outputs at 0 - 5 V

Front Panel LED Display

Switch Selectable For Channel Data Or Address

1.2 Setup and Installation

The IS10A is a single width CAMAC module using only the standard CAMAC dataway card edge connection to the CAMAC crate and controller module. The IS10A complies entirely with the IEEE 583-1975 CAMAC standard and can be installed at any CAMAC I/O station.

CAMAC modules should be inserted in the CAMAC crate only after turning off the power to the crate. Otherwise, damage to the module is possible due to momentary misalignment of pins on the card edge connector.

To insert the IS10A in the CAMAC crate, choose a convenient I/O station and slide the module into the crate with its top and bottom metal rails mated to the guide rails of the crate. Be sure that the module is properly aligned with the card edge connector at the back of the crate. Push the module toward the back of the crate with gentle pressure, but do not insert entirely. Start the threading of the front panel jack screw. Press the IS10A into the crate completely with firm pressure on the top and bottom of the front panel. Complete the threading of the front panel jack screw.

It is recommended that the IS10A module and CAMAC controller be installed alone in the crate until the user is familiar with IS10A operation enough to integrate it with other modules in a CAMAC instrumentation system. Software is included with the IS10A for stand alone operation in a Data Design SCSICrate™ Integrated CAMAC Crate and Controller. If a SCSICrate™ is to be used in the instrumentation system, this software provides an easy way to review IS10A features and to bring the module up and running quickly. The module is easily operated from two signal generator outputs with one connected to the *Cycle Start* input and the other connected to the event source input. The *Cycle Start* signal should be issued at a rate slower than the time required to complete an entire integration cycle based on the number of channels selected and the selected dwell time.

2 IS10A CONTROLS AND INTERFACES

The IS10A is a single width CAMAC module designed for access to all of its measurement interfaces through front panel connectors. These features are described on the following pages.

2.1 Front Panel Inputs and Outputs

2.1.1 Cycle Start Input

The *Cycle Start* input is used to start the integration cycle beginning at channel zero. The integration terminates when the maximum channel address is reached and the system enters an idle mode. The *Cycle Start* must be issued for each integration cycle. This is a rising edge active TTL level input and is internally terminated in 470 ohms.

2.1.2 Channel Increment Input

The *Channel Increment* input is a timing signal used to advance the channel when external dwell time operation has been selected via the CAMAC dataway. This is a rising edge active TTL level input and is internally terminated in 470 ohms.

2.1.3 Subtract Enable Input

The *Subtract Enable* input is an active high signal used to specify that the current event count should be subtracted from the accumulated total. With no input (or zero volts applied), the IS10A arithmetic unit is in the add mode. With a logical "1" TTL level signal applied, the subtract mode is selected, causing the channel accumulated count to be diminished by the value in the dwell counter. This is an active high TTL level input and is internally terminated in 470 ohms.

2.1.4 TTL And NIM Event Inputs

The event inputs serve as the interface between the IS10A and the event source. The signal supplied to the NIM input is typically the output of a discriminator or shaper. It should be conditioned so that ringing is minimized to prevent false or double counting. The minimum pulse width to ensure reliable counting is 1 ns. The NIM input is internally terminated to ground through 50 ohms. The TTL input serves as the interface to systems with TTL level outputs and is internally terminated to ground through 470 ohms. When using the TTL input at high signal rates, it is a good idea to add further appropriate termination to the input signal close to the connector. This will minimize reflections from the input connector to the external discriminator. The TTL input is generally used only at lower event rates or in situations where the distance to the signal source is short. The two inputs *can not* be used at the same time as unpredictable operation may result. The unused input should be left unconnected.

2.1.5 X And Y Analog Display Outputs

The X and Y outputs are analog signals representative of the channel memory address and accumulated counts. They can be connected to an X-Y monitor or to the horizontal and vertical channels of an oscilloscope in X-Y mode to view the accumulated count as it is being integrated. They can also be used to view the stored data when the IS10A is placed in DISPLAY mode. The X output swings 0 to 5 volts as the channel memory address is incremented from channel zero to the established maximum channel. The Y output swings 0 to 5 volts depending on the accumulated counts in each channel memory location. The counts per volt resolution is set by CAMAC command as described in section 3.3.4 below.

2.2 Front Panel Channel Address/Counts Display

The front panel LED column display indicates either the accumulated counts for each channel or the current channel address. The front panel selector switch just below the display is used to set the mode of the display. The display presents a binary number where the top most LED represents the most significant bit of the number being displayed and the lowest LED represents the least significant bit.

The counts display is useful for visually observing the integration for a qualitative determination of correct total counts. As the accumulated counts increase, higher LED's will light. The address display indicates which channel is currently addressed. When the IS10A is placed in the READ mode, the address display may be incremented slowly by the application of successive *Read Memory* (F<0>) commands to observe correct operation of the instrument. Moreover, the channel address display can be used as an indicator that the *Cycle Start* signal has been received when the number starts to increment, as an indication of integration progress in the case of long dwell time setups, or as an indication of how many channels are being used by observing the display just before the address clears to zero.

3 IS10A CAMAC OPERATION

The IS10A may be interfaced to an external host computer through the CAMAC dataway and installed controller. The CAMAC control functions are used to reset, configure, and read data from the IS10A. This section discusses operation of the IS10A through the CAMAC dataway including the function of global CAMAC signals and module specific commands.

3.1 CAMAC Global Signals

3.1.1 CAMAC Status Lines

- Q - The Q signal is active in READ mode when the addressed channel memory location contains valid accumulated count data. Q is also active as a response to the *Request LAM Status* command if an arithmetic overflow has occurred on any channel.
- X - The X signal is active as a response to every command, indicating that the module is present.
- L - The L (LAM) signal is generated when an arithmetic overflow occurs on any channel. It may be enabled and disabled by command. By default and after reset, LAM is disabled. In either case, its actual internal status may be returned on Q with the *Request LAM Status* function code.

3.1.2 CAMAC Control Lines

- I - The CAMAC inhibit line is used to effectively shut off the module to both external count events as well as *Cycle Start* inputs. As soon as the inhibit line is deasserted, the module will respond to external inputs.
- Z - The CAMAC clear cycle clears all user parameters to zero. For example, dwell time is set to a 250 ns internal signal and the maximum channel is set to zero. The internal arithmetic overflow LAM is cleared. CAMAC LAM (L) generation is disabled. All current cycles stop and the IS10A is set to the READ mode.
- C - Same as Z

3.2 CAMAC Command Summary

COMMAND	FUNCTION	SUBADDRESS	DATA
READ MEMORY	F<0>		R<Channel Count>
TEST LAM STATUS	F<8>		
RESET LAM REQUEST	F<10>		
SELECT DISPLAY RESOLUTION	F<11>	A<0 - 7>	
ENABLE READ MODE	F<12>		
ENABLE DISPLAY MODE	F<13>		
ENABLE COUNT MODE	F<14>		
CLEAR MEMORY	F<15>		
SET INTERNAL CHANNEL DWELL TIME	F<16>	A<0>	W<0> = 250 ns W<255> = 64 μ s
SELECT EXTERNAL DWELL TIME	F<16>	A<7>	
SELECT MAXIMUM CHANNEL NUMBER	F<20>		W<0 - 32767>
SET CHANNEL ADDRESS	F<22>		W<1 - 32767>
DISABLE LAM	F<24>		
ENABLE LAM	F<26>		

Note: F<16>A<6> is reserved for factory calibration.

3.3 CAMAC Command Descriptions

3.3.1 Read Memory (F<0>)

The IS10A must be in READ mode to execute this command. See the *Enable Read Mode* command below. When the IS10A is in READ mode, the *Set Channel Address* command is used to establish the first channel to be read. When the *Read Memory* command is issued, the data from the then addressed channel will be read to the dataway and the address will be incremented to the next channel. If the data read is valid channel count data, the Q signal will be true. If the data read is beyond the established maximum channel, the Q signal will be false.

The *Read Memory* command is typically used to read count data from the IS10A after a period of integration. To do this, set the IS10A to the READ mode using the *Enable Read Mode* command. Note that if data is available, *Enable Read Mode* will respond with a true Q signal. If the Q signal is false, the IS10A may be in the middle of an integration cycle or other cycle and unable to change modes. The mode will change at the end of the integration cycle. An *Enable Read Mode* command returning a true Q will indicate that the cycle is complete and the read may begin. The *Set Channel Address* function is then typically issued to point to the desired first channel. The first channel defaults to zero, but it is good practice to set it anyway. The *Read Memory* function may then be issued to read data from the first channel and increment the address to the next channel. The Q signal will be true if the data read are valid count data. By this design the *Read Memory* command may be issued in standard CAMAC *Stop on Q False* block read functions supported by most controllers. When the read is complete, the channel address should be returned to zero by issuing the *Set Channel Address* command with W<0> to ready the module for the next cycle in any mode.

3.3.2 Test LAM Status (F<8>)

A LAM signal exists internally to the IS10A which when active indicates that the accumulated count in at least one channel has incremented beyond the maximum 16,777,215 counts, a condition known as arithmetic overflow. The *Test LAM Status* command will return the status of this internal signal as a Q status signal. If Q is true upon issuing this command, the LAM signal is active and an arithmetic overflow has occurred.

3.3.3 Reset LAM (F<10>)

When the internal LAM signal is active (see section 3.3.2 above) it will remain active until reset by the *Reset LAM* command. When host software has acknowledged and handled the overflow condition the *Reset LAM* command is typically issued to enable detection of future overflow events.

3.3.4 Select Display Resolution (F<11>A<0 - 7>)

The *Select Display Resolution* command sets the scale of counts per volt presented on the Y output. The function actually assigns a range of bits to be displayed from the full 24-bit count value. The subaddress selects the range as follows.

A<0>	R2..R10	102.4 Cnts/V	≈	1000 Cnts FS
A<1>	R5..R13	819.2 Cnts/V	≈	8000 Cnts FS
A<2>	R8..R16	6553.6 Cnts/V	≈	64000 Cnts FS
A<3>	R11..R19	52428.8 Cnts/V	≈	512000 Cnts FS
A<4>	R13..R21	209715.2 Cnts/V	≈	2000000 Cnts FS
A<5>	R14..R22	419430.4 Cnts/V	≈	4000000 Cnts FS
A<6>	R15..R23	838860.8 Cnts/V	≈	8000000 Cnts FS
A<7>	R16..R24	1677721.6 Cnts/V	≈	16000000 Cnts FS

3.3.5 Enable READ Mode (F<12>)

In order to read accumulated count data from the IS10A channel memory, the IS10A must be in the READ mode. The IS10A is set to READ mode using the *Enable Read Mode* command. Note that if the command is successful and data is available, *Enable Read Mode* will respond with a true Q signal. If the Q signal is false, the module may be in the middle of an integration or other cycle and unable to change modes. The mode will change at the end of the cycle. The *Enable Read Mode* command may be issued multiple times until a command returning a true Q indicates that the cycle is complete and the read may begin.

3.3.6 Enable DISPLAY Mode (F<13>)

The IS10A is set to DISPLAY mode by the *Enable DISPLAY Mode* command. This is considered to be the idle state of the IS10A. In DISPLAY mode, the IS10A addresses each channel in sequence up to the established maximum channel. The count data are presented as an analog signal on the Y analog display output with a volts per count resolution set by the *Select Display Resolution* command. The current channel memory address is presented as an analog signal on the X analog display output with the full sweep covering channel zero to the established maximum channel. These two signals can be connected to an X-Y display or oscilloscope in X-Y mode to display a histogram of accumulated counts versus channel number.

The DISPLAY mode is the idle state where stored count data can be observed without accumulating more counts or reading the data to a host computer. The DISPLAY mode will not be entered until the current cycle of any other mode is complete. Note that the analog display is also available in the COUNT mode where the accumulation of counts can be observed. In the COUNT mode a ghost signal will tend to appear on the display before channel zero and should be ignored.

3.3.7 Enable COUNT Mode (F<14>)

The IS10A is set to COUNT mode by the *Enable COUNT Mode* command. In this mode, the IS10A waits for a *Cycle Start* signal to begin the integration cycle. When the cycle is started, the IS10A begins counting events from the event signal input in the first high speed 16-bit dwell counter. After the expiration of the dwell time as controlled by an internal or external signal, the IS10A switches to counting in the second high speed 16-bit dwell counter while adding the first 16-bit count into the first channel memory location. Switching between dwell counters in this “ping-pong” design allows very fast switching between channels with less than 2 ns latency. The process continues until an accumulation has been made in all channels up to the established maximum channel. At that point the IS10A waits for the next *Cycle Start* input signal. Note that while in the COUNT mode, the IS10A will respond to commands only while waiting for a *Cycle Start*. It will respond to the last issued command (including mode change) when the cycle is completed and the wait for *Cycle Start* has begun.

3.3.8 Clear Memory (F<15>)

The IS10A channel memory is cleared by the *Clear Memory* command. This command writes a zero to each channel memory location up to the established maximum channel. The channels are cleared in write cycle which repeats until a mode change command is issued. The IS10A will not respond to other commands until the cycle is complete. A new command issued during the cycle will be executed after the cycle is complete.

3.3.9 Set Internal Channel Dwell Time (F<16>A<0>W<0 - 255>)

The *Set Internal Channel Dwell Time* command establishes the internal source as the channel increment signal to be used during the integration cycle and specifies the dwell time between channel increment signals. The dwell time is specified as an 8-bit number (0 to 255) on W<1.8>. A specification of W<0> corresponds to 250 ns. Higher numbers add the specified number of 250 ns intervals to the dwell time. For example, a specification of W<1> corresponds to 500 ns on up to W<255> which corresponds to 64000 ns (64 μ s).

3.3.10 Select External Dwell Time (F<16>A<7>)

The *Select External Dwell Time* command establishes the external signal at the *Channel Increment* input as the signal to be used during the integration cycle to control the dwell time between channels. The dwell time controlled in this way can be any period greater than 300 ns and is not limited in any other way. In fact, the dwell time does not even need to be constant from one channel to the next or have a period divisible by 300 ns. However, it is up to the user to ensure that the dwell counter will not overflow during the dwell time. This overflow would be undetectable and occurs if greater than 65535 events are received during one dwell interval.

3.3.11 Select Maximum Channel Number (F<20>W<0 - 32767>)

The *Select Maximum Channel Number* command establishes the channel number considered to be the highest channel in the cycle executed in all modes and functions of the IS10A. This is the established maximum channel addressed during the integration cycle, the maximum channel address indicating valid data in the READ mode, the highest channel address displayed on the X analog display output, and the highest channel address cleared by the *Clear Memory* command. This function should be issued after power on or reset of the IS10A and CAMAC crate. The default maximum channel is zero. After this command is issued, the *Clear Memory* command should be issued to clear any bogus data in the newly available channel memory locations.

3.3.12 Set Channel Address (F<22>W<0 - 32767>)

The *Set Channel Address* command sets the channel memory address to a particular channel. This function is only significant in the READ mode. It is typically used to set the channel memory address to the desired channel before reading data from the module. The default address upon entering READ mode is channel zero; but, it is good practice to set the channel address before reading data, even if not required. When the read operation is complete this command must be issued with W<0> to return the channel address to zero for future cycles in any mode.

3.3.13 Disable LAM (F<24>)

The *Disable LAM* command prevents the internal arithmetic overflow LAM signal (see section 3.3.2 above) from issuing a CAMAC LAM (L) signal.

3.3.14 Enable LAM (F<26>)

The *Enable LAM* command allows the internal arithmetic overflow LAM signal (see section 3.3.2 above) to issue a CAMAC LAM (L) signal when true.

4 IS10A OPERATING EXAMPLE

The following is a step by step discussion of the typical process for gathering event count data with an IS10A. While it does not cover any specific experimental setup, it does provide a guideline to follow when interpreting the significance of IS10A inputs, controls, modes, and functions.

Step 1 Power Up and Initialization

Insert the IS10A in a CAMAC crate, turn on the power, and initialize the module by executing an initialize (Z) CAMAC cycle.

Step 2 Set Maximum Channel Number

Command Format: F<20>A<0>W<0 - 32767>

This command sets the desired number of channels to be used for the particular application. The legal values for the maximum channel number are 0 to 32767. A maximum channel of 0 is not a useful setting.

Step 3 Clear Memory

Command Format: F<15>

This command clears the memory contents from channel zero to the maximum channel number specified at step 2. The channel memory should always be cleared after power up to ensure that the integration of counts will begin from zero. Note that the *Clear Memory* command sets an operational mode which will stay active until a standard mode (COUNT, READ, or DISPLAY) is selected.

Step 4 Set Channel Dwell Time

Command Format: F<16>A<0>W<0 - 255>

This command selects the channel advance signal to be internally generated with a dwell time of 250 ns to 64 μ s. To select the use of an external channel advance signal through the *Channel Increment* input on the front panel use the command format F<16>A<7> instead.

Step 5 Start Integration

Command Format: F<14>

Integration is performed by setting the IS10A to COUNT mode and accumulating dwell counts over several cycles. Before enabling COUNT mode, all input signals should be connected and terminated as required. Two inputs are essential: the event input with a rate from DC to 1 GHz and the *Cycle Start* trigger input with a period greater than the product of the maximum channel

number and the channel dwell time. If the external dwell time has been selected, a signal source should also be connected to the external *Channel Increment* connector. After connecting these signals, the *Set COUNT Mode* command is issued to the IS10A. The integration of dwell counts over cycles will continue until the mode is changed again to DISPLAY or READ or a *Clear Memory* command is issued. The mode change will not occur until the maximum channel is reached in the current integration cycle.

Step 6 Check Overflow

Command Format: F<8>

The channel memory accumulates 24-bits per channel. For most experiments, the overflow condition will never occur. However, with fast event rates or long integration periods, an overflow may occur. To check the status of the overflow, check the status of the internal LAM signal. If an overflow has occurred the *Test LAM Status* (F<8>) command will return a true Q signal.

Step 7 Set DISPLAY Mode

Command Format: F<13>

Sending this command terminates the integration and causes the IS10A to enter the DISPLAY mode. In this mode the memory address is cycled from channel zero to the maximum channel established in step 2 with the count data and channel address being presented in analog form on the Y and X outputs respectively. This mode allows a histogram of stored counts versus channel number to be displayed on an X-Y monitor or oscilloscope in X-Y mode.

Step 8 Enable READ Mode

Command Format: F<12>

Setting this mode allows data from the IS10A to be read into a host computer over the CAMAC dataway using the *Read Memory* (F<0>) command. If the IS10A has successfully entered read mode, the F<12> command will return a true Q signal. Each successive F<0> command will increment the channel address. A true Q signal will also be returned until the maximum channel number specified in step 2 is reached.

Normally the data read cycle begins at channel address zero which will be selected when the READ mode is entered. If another address is desired, it may be preset by sending command F<22>D<0 - 32767>. After the readout has been completed the memory address should be set to zero by sending the F<22>W<0> command to allow proper operation of the cycle in any mode.

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