# APP0101: A Parallel Approach To Serial ADC On The TM1000

## 1.0 Background

It's a common problem to design a data acquisition system containing several analog to digital converter (ADC) chips. If these chips have a serial interface, the designer is faced with the prospect of a complicated hardware interface or the ordeal of designing a microcontroller and related software onto the module. Moreover, such constraints may make it difficult to sample multiple signals simultaneously. Fortunately, it doesn't have to be so difficult. This note shows a simple, albeit slow, way to sample and read several serial ADC chips in parallel with minimal additional circuitry and no module local software. This approach can also be applied to digital to analog (DAC) circuitry.

## 2.0 A Parallel Approach

Most serial ADC devices have three control signals including enable/convert, data read clock, and data. The physical form and protocol may vary, but the basic terms will be similar. The trick to reading multiple devices on a parallel interface is to realize that there is no reason why each bit of parallel data read needs to contain data from the same source. This is the only outside-the-box inspiration that is required, everything else is straightforward.

The TM1000 interface is ideal for this approach because the data written on the interface remains present after the write operation is complete. Use of this fact does require abandoning the powerful function coding features of the TM1000 and using the interface as simple I/O, but if the converter array is all the logic there is on the module then this is an acceptable compromise.

Use the TM1000 WRDATA signals to enable the converters and start conversions. Using one WRDATA signal for each converter allows converters to be addressed separately if required. A single WRDATA signal can also be used to enable all converters, but external buffer/driver circuitry may be required depending on the number of converters addressed. In the same way, the converter clock lines can be connected to one or more WRDATA signals. Connect the converter data lines to the TM1000 RDDATA signals, one for each converter. It is not hard to imagine a host software application which creates a clock edge on all or a subset of converters and reads resulting bits from the RDDATA port. The bits are separated at the host by interpreting the RDDATA word as up to 16 serial streams which are assembled into the resulting conversion values.

## 3.0 Who Would Do This?

The question better asked is why not do this? If you don't need a lot of speed and don't have any other interfaces, then this approach goes a long way toward reducing parts count, and thereby reducing cost and increasing reliability. As an example, the Data Design VM1010 four channel volt meter module uses exactly this approach.