

**DG11A
DIGITAL DELAY
GENERATOR**

1999

**DATA DESIGN CORPORATION
7851-A Beechcraft Avenue, Gaithersburg, Maryland**

DG11A GENERAL DESCRIPTION

The DG11A Digital Delay Generator is a CAMAC module designed to furnish four precisely timed delay outputs, when triggered from an external input. The timed delays are all multiples of 10 nsec, and may be as long as 167.77216 msec (24 bits). A jumper setting on the DG11A permits dividing the main clock rate by ten permitting all delay times and pulse width settings to be ten times the selected setting. The delayed outputs may be selected by a switch setting to produce one of three different pulse widths. Also, a transition at the delay time setting may be selected. With this selection, the output stays high until externally reset by rearming the unit. In addition, channels 1,2 and 3,4 may be jumper selected to provide outputs which have precisely timed start and stop times. In this case channel 1 or 3 would determine the start time and channel 2 or 4 would determine the stop time. The outputs of the DG11A are 5 V in amplitude and will drive 3V into 50 Ω lines. A front panel input provides the external trigger input to the DG11A module. This input is positive edge triggered and is not internally terminated, so that the trigger input may be routed to several modules in a daisy chain connection.

The accuracy of the timing within the DG11A module is based upon an internal 10 MHz crystal oscillator. This oscillator phase locks a triggerable 100 MHz LC oscillator from which the 10 ns output period is used to provide the resolution of the instrument. The LC oscillator has the phase agility to resynchronize itself to the applied front panel trigger input. As a result, the timing jitter measured from the application of the trigger input to the delay outputs is less than 1 ns rms for delay times up to 10 ms.

The DG11A is designed to receive all commands via the CAMAC dataway. The delay for each channel is programmed through the dataway. The internal architecture of the DG11A provides eight tables of delay programs; each program containing delay settings for all four channels. Thus, it is possible to change the delays on all four channels by just changing the active table. All data written to and read from the DG11A uses the active table. The memory containing all of the delay values can be transferred to a nonvolatile memory, so that the data written to the module will remain even after the crate power is switched off.

As a failsafe against accidental firing, the DG11A must be in an armed state prior to responding to a front panel trigger input or dataway trigger command. An auto-arm mode may be used if the failsafe feature is not needed. In this case, the DG11A may be fired at a rate that depends only on the longest programmed delay time.

The DG11A module is a single width CAMAC module conforming to IEEE standard 583-1975. It derives all necessary operating power from the crate, and electrical interfaces via the dataway. It has the capability for local manual control using a companion module DG12. This module provides thumbwheel switch entry of delay settings to the DG11A. Up to eight DG11A modules in a single crate may be operated by a DG12.

In high electrical noise environments, or where high isolation is desired, an Optical Fiber Interface module may be used with the DG11A. This interface consists of an electrical to optical converter which plugs into the front of the DG11A and has four optical fiber outputs. This unit is powered only from the output pulses of the DG11A. A receiver module for each channel converts the optical signals back to electrical signals. The receiver module may be located up to 300 meters away.

DG11A SPECIFICATIONS

Inputs

Trigger input to initiate delay; 2.5V min

Input Impedence

470 Ω last module in daisy chain
should be terminated in 50 Ω

Timing Resolution

10 nsec; maximum delay is 167.77216 msec.
100 nsec; maximum delay is 1.6777216 sec.

Timing Jitter

less than 1 nsec rms from external trigger
for delay less than 10 msec. Less than 4nsec
for delay less than 167 msec

External Clock Input

10.0 MHz input used to synchronize
multiple DG11A modules; 2V min.

Ext Clock Impedence

470 Ω last module in daisy chain
connectors should be terminated in 50 Ω .

Local Enable Input

Provides local entry of DG11A data
via DG12 module.

Aux Output Mode

Channel 1,2 or channel 3,4 may be strapped
to provide presettable start/ stop time.

Indicators

LED indicators for table selection, armed status,
LAM status.

Package Size

Single Width CAMAC (IEEE 583)

CAMAC Interface

Delay selection W1,...,W24
Delay readout R1,...,R24
Table selection/Channel A1,A2,A3
Armed condition/LAM status on Q
LAM after last channel delay

Operating Power

+6v 1.5 A
-6v 1.8 A
+24v 50 mA
-24v 50 mA
All power supplied by CAMAC crate

Outputs

5V from 50 Ω on four Lemo connectors

Output Pulse Width

DIP switch selectable widths for
each channel: 200 nsec, 2.5 usec, 40 usec .
Also selects level change until reset.

COMMAND SUMMARY

COMMAND

CODE

Read Delay Data	F<0> *A<0...3>
Read Armed Status	F<7>
Read LAM Status	F<8>
Remote Trigger	F<9>
Reset LAM	F<10>
Arm Module	F<11>
Non Volatile Store	F<12>
Select Table	F<13>*A<0...7>
Auto Arm Enable	F<14>
Write Delay Data	F<16>*A<0...3>
Disable LAM	F<24>
Restore Default Data	F<25>
Enable LAM	F<26>

DG11A OPERATION

Module Preparation

Before inserting the DG11A module into the CAMAC crate, the DIP switch should be set to select the desired output pulse width for each channel. The available pulse widths are 200 nsec, 2.5 usec, or 40 usec (2 usec, 2.5 usec and 400 usec when the resolution select jumper is in the 100 nsec position). Each pulse width setting is independent from the others so each channel may have a different pulse width. Also programmable by a switch selection is a level change from 0V to 5V at the desired delay time. This level will remain set until the DG11A is rearmed. An alternate output mode is available in which channel 1 (or 3) will be set at the delay time programmed into that channel, and will be reset at the delay time programmed into channel 2 (or 4). If this mode is used for channel 1 (or channel 3), it is important set the DIP switch for channel 1 (or 3) to the high to rearm (both switches "on") position. In the selectable start/ stop time mode, channel 2 (or 4) continues to operate normally so the pulse widths for these channels may still be programmed by the switch setting for those channels. Refer to the DG11A DIP switch selection illustration on the DG11A printed circuit board. Make sure that the power is switched off before attempting to plug the DG11A module into the crate; otherwise damage to the module may result from a momentary misalignment of the connector pins.

Interconnection of the DG11A module

The DG11A module has Lemo connectors on the delayed outputs which should be connected to external equipment via 50 Ω coaxial cables and terminated in 50 Ω for minimum reflection. The signal level on the delayed outputs is 5V open circuit and will supply a minimum of 2.5 V into a properly terminated load. The trigger input impedance is high, so that multiple DG11A modules may be driven by the same trigger source in a daisy chain connection. The last module in the daisy chain should be terminated in 50 Ω . The trigger source must provide at least 2.5V into 50 Ω , and should have a rise time less than 5 ns for minimum trigger jitter. If the external clock connection is to be employed to synchronize multiple DG11A's, a similar daisy chain connection technique should be employed.

Selection of External Clock

The DG11A timing chain is controlled by an internal 10 MHz crystal oscillator, having an accuracy of 0.005%. If it is desired to provide the smallest possible skew between modules, or a higher accuracy, a common clock may be applied to all of the modules via the front panel input labeled EXT CLOCK. The external clock should be a 10 MHz +/- 1% tolerance sine or square wave signal having a level of 1V to 2V rms into 50 Ω . Application of the external clock automatically disables the internal crystal oscillator.

CAMAC Operating Sequence

The delay settings for each of the four channels are sent to the DG11A module by issuing the command F<16>, with subaddress A<0,1,2, or 3> corresponding to channels 1,2,3 or 4 respectively. The data sent in this command selects a delay in integer multiples of 10 ns. It takes the DG11A approximately 10 us to properly store the data transmitted to the module by an F<16> command. During this time, no new commands should be sent. After all four delays have been received, another set may be sent after first selecting a new active table via the command F<13>, and then repeating the F<16> sequence. The default active table upon power up is table zero. As delay values are received by sending F<16> commands, they are stored in the RAM portion of the DG11A nonvolatile memory referred to as the NVRAM. If the values in this RAM are to be retained during power off time, the command F<12> should be issued. This command saves the delay values stored in all of the tables, not just the active table. Upon powering on the crate, issuing the command F<25> will transfer the data from the NVRAM into the delay table area.

It is possible to read out the delay values for the active table by issuing the command F<0> with subaddress A<0,1,2,or 3> corresponding to channels 1,2,3 and 4. This capability provides assurance of the delay for each of the channels. In addition, it provides a method of recording delays selected by the DG12 Manual Data Entry Module. In order to read out the delays, it is first necessary to set the active table to the desired one. Due to the internal architecture of the DG11A module, it is necessary to issue the read command F<0> command twice, with the same subaddress. Valid data for the selected channel exists only on the second read command.

The DG11A module must be in an Armed state before it will respond to a front panel trigger or CAMAC trigger command. The module is armed by issuing the command F<11>. The armed status is read out on the CAMAC dataway Q line during a read command, or by issuing command F<7>. After the trigger, the module will need to be rearmed. However, the unit may be set into the Auto Arm mode by issuing the command F<14> prior to firing the module. In this mode, repeated trigger commands may be sent to the DG11A at a rate that depends only on the longest delay.

The LAM service request may be enabled by sending command F<26>. The LAM may be used to indicate that the module has been triggered and has completed the longest delay time. If this feature is enabled, the LAM must be reset after each trigger command by sending command F<10>.

High Speed Operational Notes

If the DG11A is operated in a high trigger rate condition, being one in which the unit is fired as soon as it is rearmed, erroneous delay readings may result if the trigger source is running at the same time F<0> commands are being issued. Likewise, changes in delay values via F<16> commands should not be sent until the trigger source is temporarily disabled. If it is not possible to interrupt the trigger source, the module should be temporarily disabled by disarming it. Sending the command F<15>, Auto Arm Disable, will cause the unit to be disarmed after the next trigger. The module may be restored to the high speed condition by first sending the command F<14>, followed by the command F<11>.

DG11A OPERATIONAL DETAILS

Timing Resolution Selection

The DG11A has both a 10 ns resolution as well as a 100 ns resolution selection. The 10 ns setting provides a maximum delay setting of 167.77216 msec. The 100 ns resolution provides a maximum delay of 1.6777216 seconds. A jumper labeled J15 on the circuit board selects the resolution. Installing the bridging jumper on the upper pins of J15 selects the 100 ns resolution. To obtain 10 ns resolution, the jumper must be installed on the lower two pins. The output programmed width selection as described in the following section is multiplied by ten when in the 100 ns resolution setting.

Output Pulse Width Selection

The DG11A module can be configured to provide various types of outputs. In the normal pulse output mode, the DG11A will provide a pulse on each output after the preset time interval. The width of this output pulse may be one of three preset intervals; 200 ns, 2.5 us or 40 us. An eight position DIP switch is used to select the desired pulse widths for each channel. Two positions of the switch are used for each channel's width programming. A chart printed on the DG11A circuit board provides a convenient table for presetting the DIP switches. Each output pulse width may be configured independently of the others.

Another output mode may be selected in which the output is set high at the set time and stays high until the module is armed again. It will be necessary to have the Auto Arm mode disabled if it is desired to have the outputs stay high. If the Auto Arm mode is enabled, then the outputs will be reset automatically after the last output pulse, since that event will initiate the counter preset and Auto Arm sequence. This mode provides the ability to generate a level shift at a preset time, which will stay high as long as desired.

In a third output mode, the DG11A may be configured to provide two output pulses (on channel 1 and 3) with precisely timed beginning times as well as ending times. In this mode the selection of pulse ending time for channel 1 depends on the delay set into channel 2. Likewise, the ending time for channel 3 depends on the delay value set into channel 4. Using this mode any length pulse up to the maximum length of the DG11A's internal counters may be generated. The output leading edge will begin at the time preset by channel 1 (or 3). The output will stay high until the time preset into channel 2 (or 4). Note that there is no protection to prevent a smaller time value to be preset into channel 2 than channel 1. This would correspond to a pulse that ended before it began. When using this mode of operation, a pair of channels, either 1/2 or 3/4 is interconnected. The other pair may be used in the normal pulse output mode.

Use of The Non Volatile Memory Feature

The DG11A has an internal memory used for storing delay values. This device is referred to as an NVRAM, and is actually a Random Access Memory or RAM with an underlying Read Only Memory or ROM. The contents of the entire RAM may be stored at one time in the ROM, as well as be restored from the ROM. When a delay value is sent to the DG11A, that value is written into the RAM portion of the non volatile memory. The RAM has enough storage capacity to hold eight tables of delay settings. One table corresponds to a set of values for each of the four delay counters. Upon power up, the entire ROM contents are transferred into the RAM. The table selection is also preset to the table zero. As a result, the module's four delay counters will be preset to the delay settings in table zero. If new delay values are sent to the module, they will change the values stored in the RAM portion of the NVRAM. However, they will not affect the values stored in the ROM. This means that if the delay settings are changed for any or all of the seven tables, the module will appear to have new data in the memory. However, if the power is turned off, the values sent to the module will be lost. In order to make the new settings the default settings it is necessary to send the command NON VOLATILE STORE F<12>. This command writes the entire RAM contents into the ROM portion of the NVRAM. If after changing the delays in the DG11A module, it is desired to restore the DG11A to the original power up ROM values, the command RESTORE DEFAULT STATE F<25> may be sent instead of resetting power.

The delay values stored in the memory may be read through the dataway by first selecting the active table with the F<13> command. Because of the byte wide storage in the memory, it is necessary to send the read command F<0> twice. The first read command places the data for the selected channel in the 24 bit CAMAC bus output register. The data read out in the second read will be the valid delay value for that channel.

The non volatile memory and the table feature of the DG11A module permit the storage of calibration delay settings, or some other values which can effectively test the user configuration. It is reliable, requires no power, and has a data retention time measured in years.

DG11A COMMAND SUMMARY

COMMAND	FUNCTION CODE	SUB ADDRESS	DATA
Read Delay Data	F<0>	A<0,1,2,3>	R<24,...,1>
Read Armed Status	F<7>	----	Q =1 indicates armed
Read LAM Status	F<8>	----	Q =1 indicates LAM = 1
Remote Trigger	F<9>	----	
Reset LAM	F<10>	----	
Arm Module	F<11>	----	
Non Volatile Store	F<12>	----	
Select Active Table	F<13>	A<0,1,...,7>	
Auto Arm Enable	F<14>	----	
Auto Arm Disable	F<15>	----	
Write Delay Data	F<16>	A<0,1,2,3>	W<24,23,...,1>
Disable LAM	F<24>	----	
Restore Default Data	F<25>	----	
Enable LAM	F<26>	----	

Command Notes:

After an F<0> or F<16> command is sent , a wait time of 15 usec is necessary before sending the next command.

The F<0> command must be sent two times with the same subaddress to read out the stored data on the selected channel. The data received during the second F<0> command is valid.

DG11A THEORY OF OPERATION

The interval determination circuitry of the DG11A module contains four 24 bit counters, and a 100 MHz oscillator. Before application of the trigger signal, the counters have been preset to values corresponding to the selected time delays for each channel. Immediately after the trigger, pulses from the 100 MHz oscillator cause each counter to decrement from its preset value. At a time corresponding to the oscillator period (10 ns) times the counter's preset value, each counter will reach its zero state. This condition causes an underflow signal which in turn sets the delay output synchronous with the next oscillator pulse. The counters continue to count beyond this point in order to generate one of the selectable output pulse widths. DIP switches (two for each channel) are set to select one of three output pulse widths of - 200 ns, 2.5 us, or 40 us. Also, the output may be set to provide a transition which is set high at the preset delay, and stays high until the unit is rearmed. A third mode is also user selectable in which the output for channel 1 (or 3) is set high at the delay programmed into that channel, and set low after the time set into channel 2 (or 4).

Normally in a free running oscillator delay counter system, there is an uncertainty time or jitter in the time from the application of the trigger to the output. This jitter is bounded by +/- 1 oscillator period. It is caused by the variable phase of the oscillator at the instant of the trigger. In order to avoid this ambiguity, the timing circuitry in the DG11A contains a 10 MHz crystal oscillator which synchronizes a 100 MHz LC oscillator via a phase locked loop. The LC oscillator is comprised of a logic gate with a tuned feedback network feeding back to one of the gate inputs. The output of this oscillator is divided by 10 and phase detected with the 10 MHz crystal oscillator. The resultant phase error drives a varactor diode which instantaneously corrects the LC oscillator to stabilize its frequency against changes due to temperature, aging, etc. When a trigger is received, a 20 ns delay cycle is initiated. This condition causes the LC oscillator to be stopped synchronously with its next output pulse. This is accomplished by causing the other input of the LC oscillator gate to go to a logical 1 state, synchronous with its current phase. At the end of the 20 ns delay cycle, the oscillator restarts with a new phase which is now synchronized to the trigger. During this time, the phase locked loop is effectively opened, so that the loop does not attempt to recorrect the phase to its old (pre trigger) value. Instead, the initial phase error produced after the oscillator re-starts is measured, and temporarily stored using a sample and hold circuit. The phase locked loop is then reactivated; only now it will hold this phase offset value constant for the duration of the timing cycle. The result of this operation is to provide a timing clock with the stability of a crystal reference, with the instantaneous start capability to eliminate the jitter.

The DG11A contains a nonvolatile random access memory referred to as an NVRAM used to store delay parameters. The NVRAM has enough room for eight tables of delay values. The organization of the NVRAM is 128 by 8, with each delay value occupying 3 bytes (each table takes 12 bytes). At the time after the module is triggered, the set of NVRAM data values in the active table locations are loaded sequentially into the four counters one 4 bit nibble at a time. The entire reloading sequence takes approximately 40 us. A write cycle from the CAMAC dataway stores the delay parameter into both the selected counter and the NVRAM at the active table position. The contents of the NVRAM may be read out to the CAMAC dataway, if extra assurance of the programmed delay is desired. In this case, the three bytes in the NVRAM containing the delay value for the selected channel are transferred to the 24 bit output buffer at the time of the Read command. Since the buffer is read out instantaneously at the Read command, the information in the initial command will not be valid. At the second Read operation, the buffer data will contain the correct value. Transfer of data within the volatile portion to the nonvolatile portion is controlled by command.

The counter reload circuitry initiates its cycle at the a time after the last delayed output of the four channels. Also, unless the unit is in the Auto Arm mode, it will not respond to any new trigger inputs. The status of the Armed condition is read out on the Q line of the dataway as is the LAM status (which is used to indicate the end of the last channel delayed output). In the current DG11A circuit board version, the discrete counter chips and associated support logic have mostly been replaced by Altera 7032 EPLDs. Only the LSB counter chip which is designed using high speed ECL is not integrated into the EPLD. This updated design provides a lower power implementation of the DG11A and requires fewer parts.